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PL-TR-96-1112

PL-TR-96-1112

AFFORDABLE, LIGHTWEIGHT, HIGHLY CONDUCTIVE POLYMER COMPOSITE ELECTRONIC PACKAGING STRUCTURES

Composite Optics, Inc.
9617 Distribution Avenue
San Diego, CA 92121

June 1996

Final Report

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PL-TR-96-1112

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13. Supplementary Notes

14. Abstract The objective of this proposed SBIR research project is to develop the technology which will enable the production of affordable, lightweight, highly conductive polymer composite electronic packaging (i.e., electronic housings and heat sinks). The research will center on predominately polymer matrix composite materials and how various material designs can be utilized in various structural/thermal configurations to produce electronic housings and heat sinks that exceed the performance requirements of current aluminum electronic housings and metallic heat sinks (and at one-half the weight).

The applications of this technology is very suited for commercial satellites as well as aircraft avionics, shipboard and field electronic packaging. This technology has the capability to displace aluminum for thermal/structural applications.

15. Subject Terms Polymer Matrix, Multifunctional, Composites, Highly Conductive, Electronic Packaging, Snap Together, Self-Fixturing

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1.0 EXECUTIVE SUMMARY

Background

There is a definite need of research for improving the materials and fabrication techniques that are currently being utilized for the fabrication of electronics enclosures and heat sinks. The vast majority of these currently in use are fabricated from aluminum. This is due to the fact that aluminum is relatively inexpensive, easy to machine, and exhibits good thermal conductivity and EMI shielding properties.

As electronics and printed circuit cards become more powerful and compact, the additional heat that needs to be dissipated through the containment structure or electronic enclosure presents new obstacles. The additional heat and subsequent temperature swings from low to high temperature (when power is switched on and off) will decrease the reliability of these new electronic systems unless a cooling systems is utilized. Obviously, the size and weight of a cooling system will offset the reduced size and weight advantages of these new generation electronics.

Even if heat dissipation is not an issue, the use of composite materials have proven significant weight savings over traditional metal structures.

Fortunately, there are new materials and processes that have recently been developed. For example, laminates utilizing K1100 graphite fibers have 3.5 times the electrical conductivity of aluminum (in the fiber direction) and new assembly methods have been patented (SNAPSAT™) for low cost mass production of composite hardware.

Objective

We intend to investigate new materials and processes that can be utilized in the construction of a new generation of electronic enclosures and heat sinks.

More specifically, we plan to investigate: 1) the different types of materials now available, or being developed, that could potentially be used and to analyze their use in construction of an electronics enclosure or heat sink, and 2) the low cost fabrication techniques to process these materials.

Approach and Technical Challenges

The proposed plan is to take an existing design of an aluminum electronics enclosure and convert it to SNAPSAT™, flatstock design utilizing composite materials. These two designs will then be compared directly for: 1) weight, 2) strength, 3) thermal performance, and 4) cost to fabricate.

The most challenging aspect of meeting our goal to improve performance affordably is the costing element of the raw materials. Hopefully, as this technology gains approval and becomes more widespread, the number of manufacturers of these materials and the quantity demanded on an annual basis will naturally drive the price to lower levels.

Results and Payoffs

We have summarized that the composite materials reviewed under this program will significantly reduce component weight and improve thermal performance/conductivity for the electronic enclosure analyzed. The ensuing step will be to fabricate an enclosure in order to utilize this information and to test actual hardware in the Phase II portion of this SBIR.

Recommendations

An important aspect of the electronic enclosure, especially in space applications, is its ability to withstand radiation exposure. We highly recommend pursuing this area for more information regarding lightweight radiation protection.

2.0 TECHNICAL OBJECTIVES AND DISCUSSION

Task 1:
Kick-off Meeting

The first task performed on this program consisted of a team introduction and program plan discussion. The team members for this SBIR are:

Phillips Laboratory (PL) - customer,
Composite Optics (COI) - primary investigator and mechanical design,
TecMation Associates (TMA) - thermal and structural analysis.

The program plan was to select an STRV-2 design for an aluminum electronics enclosure and convert it to a graphite/polymer matrix composite design. The structural and thermal performance of the new design was then analyzed and compared to the aluminum enclosure.

Note: This program was modified after contract award to include an actual STRV-2 flight unit fabricated from the new composite design. Subsequent to the completion of the composite design, a number of STRV-2 design changes precluded the flight possibility (due to additional schedule and cost impacts). The added program funds were then removed and the program objective was returned to the original plan

Task 2:
Materials Study

P120/954-3 was the baseline material selected for the electronic enclosure analysis. This material is capable of satisfying both the thermal and structural requirements. Also, Fiberite and Amoco, both U.S. companies, have consistently provided reliable materials and support in tackling new technological challenges. Table I lists other candidate prepreg materials that could potentially be used for this type of application.

Additional materials studied consisted of P75S/954-3 used for construction of a SEM-X thermal plate. The plate was redesigned to provide weight savings as compared to the G10 original design. The result was a 33% weight reduction from the G10 board. See Figure 1 for details.

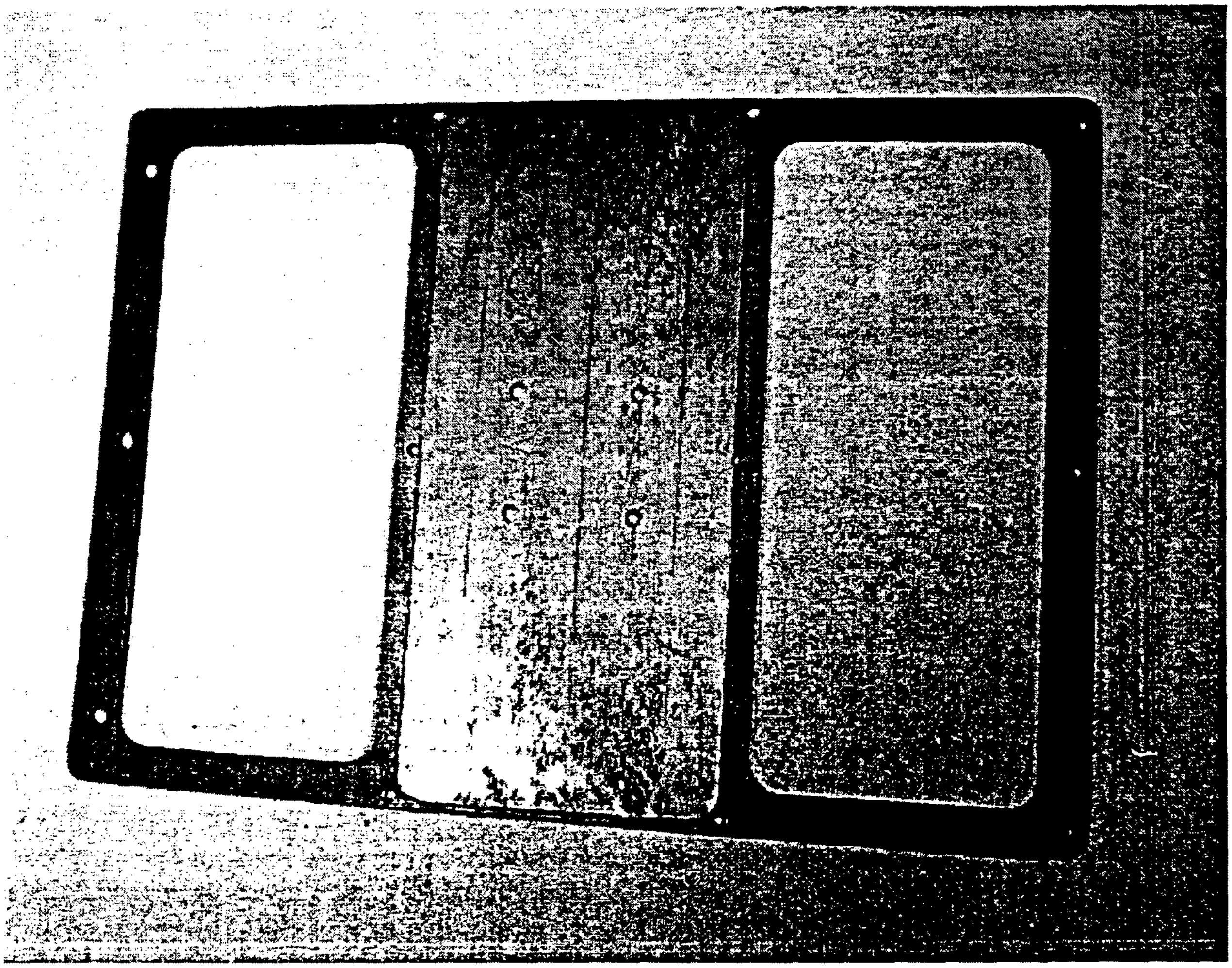
TABLE 1. Candidate Materials For Electronic Housings and PCB Heat Sinks

ELECTRONIC HOUSINGS (VME BOX)			
RAIL	*RIBS (or FIN)*	*STRUCTURE*	*RADIATOR*
K1100X/954-3	K1100X/954-3 (PMC)	P75S/954-3 (PMC)	K1100X/954-3 (PMC)
K13C2U/954-3	K13C2U/954-3 (PMC)	T50/954-3 (PMC)	K13C2U/954-3 (PMC)
P120/954-3	K13C24/954-3 + TC1050	K13C24/954-3 (PMC)	P120/954-3
(See Notes 1 & 2)	K13524/954-3 + TC1050	K1100X/954-3 (PMC)	
	P120/954-3	P120/954-3	

Notes: Table Revisions

1. PL and COI mutually agreed to eliminate aluminum extrusions.
2. Sandia thermal analysis shows graphite acceptable for rails.

Another material that was considered for the rails was a hard coating (i.e., vacuum deposited Zirconium Nitride) for the graphite card rail surfaces. This material would be applied to the area which comes into direct contact with the printed circuit boards (PCB) and would prevent the breaking of graphite fibers due to friction created from sliding PCBs into the enclosure.



Design & Fabrication by COI

Size:	211mm x 150mm x 1.0mm
<u>Configuration</u>	
Materials:	P75S/954-3Gr/CE Tape Thermograph 8000 Cond. Composite (Inlay)
Weight:	33% Reduction from G10 Board
Tested by:	Sandia Labs
Performance:	Equivalent Temperature Distribution as G10 Baseline

Figure 1. SEM-X Thermal Plate

Task 3:
Design Concepts

The STRV-2 design and requirements package is detailed in Appendix I. The composite top level design and fabrication sketches are located in Appendix II. Other significant design information is as follows.

1. Enclosure is covered on all six sides.
2. Circuit cards are per Mil-P-55110, fiberglass polyimide (.080"-.110" thick).
3. Cards are attached using Camloc type wedge clamps (90-125 lb. pressure).
4. 35 watts of power are being dissipated with a maximum of 50 watts.
5. Bottom deck contains power supply (approx. 12 watts).
6. Circuit boards utilize Mil-C-55302/57-1 and Mil-C-55302/58-1 connectors.
7. Circuit boards are 5.7" x 6.1", thickness is .080"-.100"

The design concept was maintained as a simple configuration. Additional information and requirements that would be necessary for and should be addressed for potential PMC candidates evaluation are:

1. What is aluminum panel thickness?
2. What is the card orientation in the enclosure?
3. How many PWB cards are in the enclosure?
4. What is the decibel level requirement for EMI shielding?

Task 4:
Thermal Analysis

See Appendix III - TMA final report.

Task 5:
Structural Analysis

See Appendix III - TMA final report.

Task 6:
EMI / ESD Protection

EMI/ESD protection can be achieved across the panel areas either the shield characterization of the base composite laminate or by plating methods or the application of filled paints (i.e., Electrodag). Continuity of protection across joints is critical. For interface areas where access covers are attached, wire mesh or filled rubber gaskets may be used. Corner, lap shear, and butt bond joints should be thoroughly coated using metal filled adhesives or paints at these bond joint, or in some cases, employing a joint configuration which has a non-direct, torturous path for the electron penetration.

Task 7:
Radiation Tolerance

Currently, radiation protection is a measurement that is in direct proportion to the density of the protective material being used. Radiation protection improves as the density of the protective material is increased.

At this time, current solutions to radiation protection for electronics housed in a composite enclosure consist of using radiation hardened electronics or by covering the enclosure with a tantalum foil.

There can still be a weight savings realized using these methods provided the radiation protection required is below the radiation protection offered by an aluminum, or denser, enclosure.

COI currently is investigating new potential methods (i.e., multi-layered thin films) for radiation protection and may have the opportunity to try these during Phase II.

Task 8:
Cost Analysis

Our cost estimate to fabricate an enclosure based on the Figure 1 design is $35,000. This includes: detail fabrication drawings, manufacturing travelers, materials and labor to fabricate two (2) units. Subsequent units would be much less expensive. A Rough Order of Magnitude estimate for production quantities for an enclosure comparable to this design would be:

3 - 25 units	$10,000 ea.
26 - 100 units	$ 7,500 ea.
101 - 500 units	$ 5,000 ea.

A leading contributor to the price of these enclosures is the cost of graphite prepreg. The cost of prepreg can vary from $250 per pound (i.e., M46J/954-3) to over $2,300 per pound (i.e., K1100X/954-3). The above prices include a prepreg cost of approximately $1200 per unit.

3.0 CONCLUSIONS AND RECOMMENDATIONS

We conclude that the composite materials available today offer an exciting alternative to aluminum for the construction of electronic enclosures and heat sinks. The traditional weight savings, plus new improvements with in-plane thermal conductivity, have created a new generation of materials which require further investigation and characterization. Additionally, the need to fully understand the performance of these materials is fueled by the use of more compact, higher density electronics and the heat they create. Although we do not expect the cost of composite enclosures to be quite as low as aluminum, we expect the future will allow for a higher cost due to the value added qualities of these materials. Also, as the benefits are realized and the demand for these enclosures increases in the future, we expect the raw material and fabrication prices to decrease.

Our recommendation is to continue the study of these materials and to apply them in practical applications where hands-on design, analysis, and testing will better define their capability and cost. As of this writing, we have just begun Phase II of this SBIR -- Mightsat II.1 spacecraft design and analysis. This spacecraft has a specific need for lightweight, highly conductive materials for thermal management around a Pulsed Plasma Thruster and other electronics. This provides an excellent opportunity to take advantage of the information gathered under Phase I and to expand our knowledge of these materials to determine how they can be effectively applied to a spacecraft structure.

PL Qualification Test Random Vibration

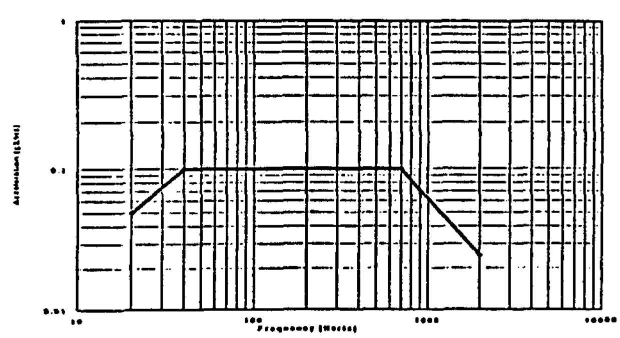
Objective - Demonstrate the ability of VISS to withstand ascent loading conditions

Note: The following specifications reflect only PL testing requirements. Total VISS testing requirements are specified in detail in the VISS Testing Requirements Document.

Test Specifications -

- Orthogonal test axes:
  - normal to VISS baseplate (X axis)
  - along MWIR's line of sight (Z axis)
  - orthogonal to X and Z axes (Y axis)
- Excitation time per axis: 2 minutes
- Spectral level: Profile specified in JPL's System Requirements Report (Para. 3.4.6.2.6.1, Fig. 3-1(b))

Random Vibration Spectral Profile



Frequency Range	PSD (g^2/Hz)	Max Control Bandwidth	Tolerance
20 Hz	0.05	10 Hz	± 1.5 dB
20-40 Hz	+3.0 dB/octave slope	10 Hz	± 1.5 dB
40-700 Hz	0.1	37 Hz	± 1.5 dB
700-2000 Hz	-4.0 dB/octave slope	100 Hz	± 3.0 dB
2000 Hz	0.025	100 Hz	± 3.0 dB

The overall acceleration level is 11.4 grms.

PL Qualification Test Random Vibration (cont)

Success Criteria:

- No leakage or buckling of bellows (visual inspection)
- Structural integrity of VISS intact (visual inspection)
- Open loop transfer functions (72) comparable to baseline transfer functions

PL Qualification Test Thermal Vacuum

Objective - Demonstrate the ability of VISS to withstand a combined extreme vacuous and thermal environment. The test will allow for detection of design, material, manufacturing, and workmanship defects.

Note: The following specifications reflect only PL testing requirements. Total VISS testing requirements are specified in detail in the VISS Testing Requirements Document.

Test Specifications -

- Number of cycles: 2
- Temperature range: -36°C to 31°C
- Temperature rate: 1°C/min < avg rate of change < 2°C/min
- Pressure level: 10^{-4} Torr

PL Qualification Test Thermal Vacuum (cont)

Test Specifications -

- Rate of pressure drop: 1 psi/sec
- Thermal soak: first and last thermal cycles (8 hrs)
- Tolerance: temperature: ± 3°C
  pressure: no higher than 10^{-4} Torr and no lower than 10^{-6} Torr

Success Criteria -

- VISS electronics start-up @ hot and cold temperature extreme down to 10^{-4} Torr
  - Exposure test of electronics to determine health status of DSP, A/D, D/A, 1553, RAM, EEPROM, and provide info on gross sensor failure and the current feedback on the voice coil drivers

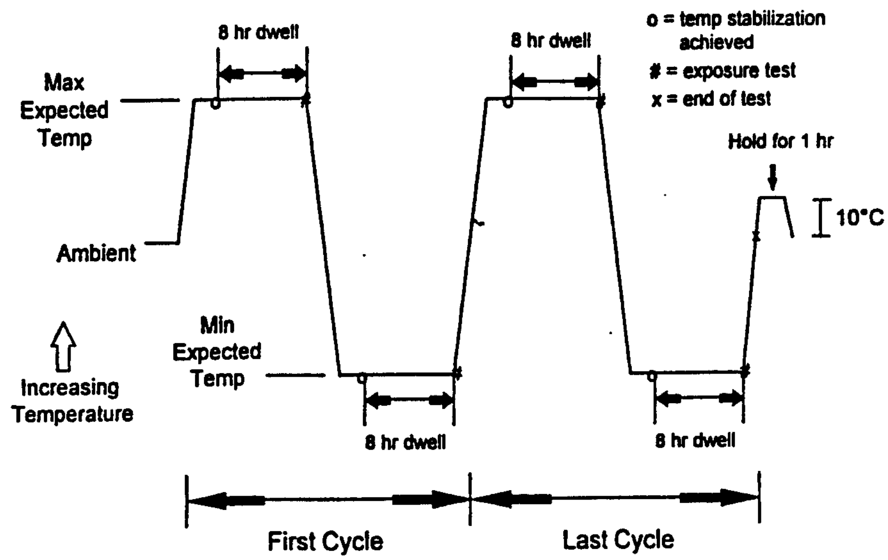
PL Qualification Test Thermal Vacuum (cont)

Success Criteria -

- Open loop transfer functions (72) comparable to baseline
- Structural integrity of VISS intact (visual inspection)
- No leakage or buckling of bellows (visual inspection)

Thermal Vacuum test will also satisfy bake out requirements

PL Qualification Test Thermal Vacuum Profile



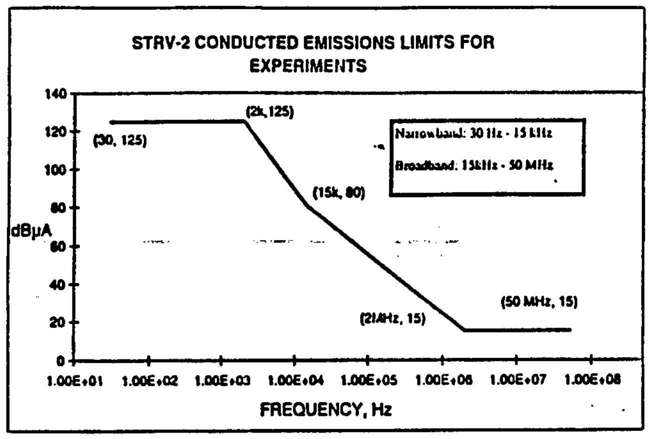
PL Qualification Test Electromagnetic Compatibility

Objective - Demonstrate VISS electromagnetic compatibility compliance with JPL's System Requirements Report

Testing Measurements -

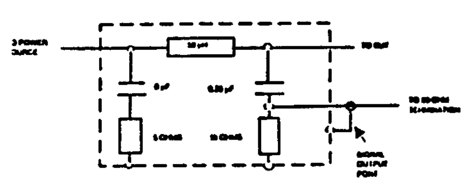
- DC Isolation
  - DC resistance check of VISS interface end circuits to verify that they are isolated from chassis ground
  - Performed prior to application of power to VISS
- Conducted Emissions
  - Ripple:
    - » VISS frequency domain emissions on the DC power lines are measured
    - » A line impedance stabilization network (LISN) is required for measurements and defined in JPL's System Requirements Report

Conducted Emissions Limits

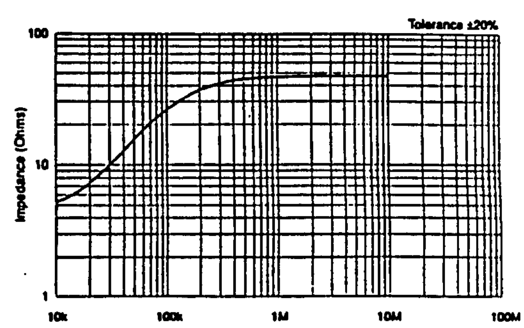


Line Impedance Stabilization Network

Schematic



Impedance Characteristics



PL Qualification Test EMC (cont)

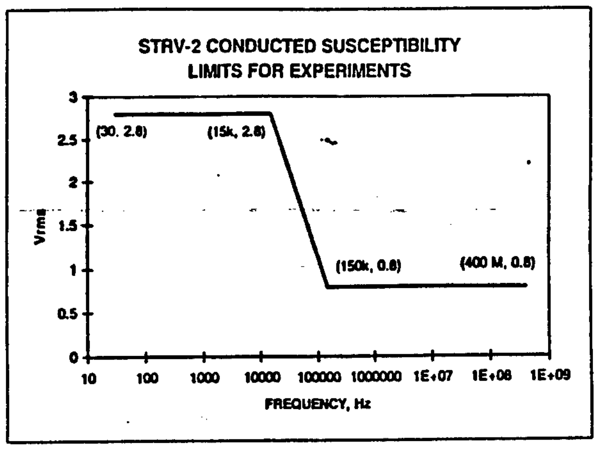
Testing Measurements -

- Conducted Emissions
  - Transients:
    - » VISS initial, in-rush current that appears on the primary bus at turn-on is not to exceed 10 amperes
    - » VISS operational transients after initial turn-on are not to exceed 1.5 times the steady-state current
    - » VISS voltage transients on the power lines are not to exceed ± 18 volts
    - » VISS voltage surges, due to load switching, are not to exceed ± 6 volts
- Conducted Susceptibility
  - Ripple Voltage:
    - » For frequencies below 250 kHz, an injection transformer is used to apply the signal
    - » For frequencies above 250 kHz, a 1microfarad capacitor with a series inductor is used to apply the signal

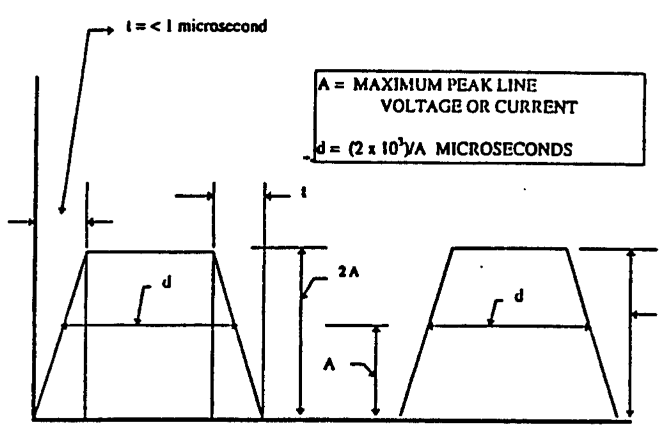
PL Qualification Test EMC (cont)

- Conducted Susceptibility
  - Transients:
    - » VISS tested for susceptibility to pulse transients induced on the power lines
    - » Repetition rate shall be 2 pps
    - » Product of the pulse width at the 50% points shall be such that the product of the pulse width and peak amplitude is 4×10^{-3} volts (or amperes)
    - » Signal is applied using an injection transformer
- Radiated Emissions
  - Electric Field:
    - » VISS electric field emission is characterize
    - » Testing is conducted in an EM shielded chamber with VISS connected to its support equipment with "flight-like" cabling and operated in its most active mode (i.e.. active isolation, suppression, and steering)
    - » Only narrowband measurements are required

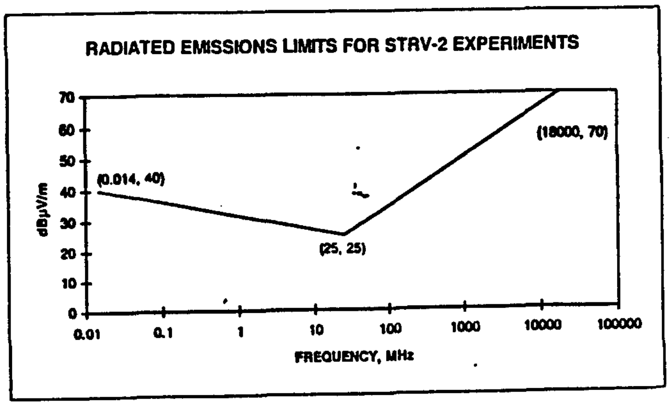
Conducted Susceptibility Limits (Ripple)



Conducted Susceptibility Limits (Transients)



Radiated Emissions, Electric Field Limits (Narrowband)

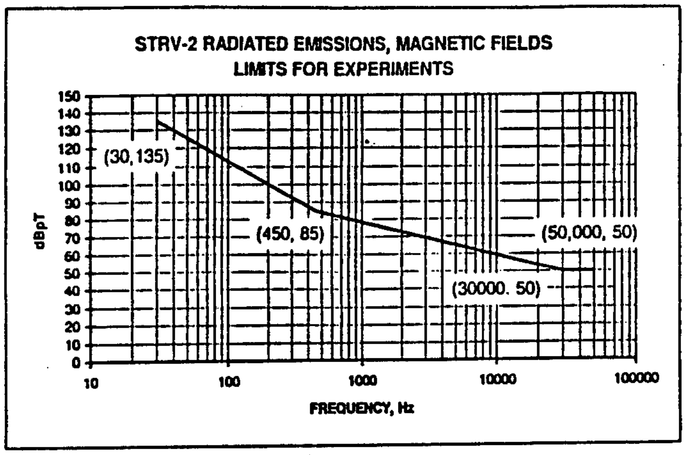


These limits will be notched at the telecommunications frequencies once the S/C and launch vehicle are defined

PL Qualification Test EMC (cont)

- Radiated Emissions
  - AC Magnetic Field:
    - » VISS magnetic field emission is characterized
    - » Measurements are similar to electric field measurements except for the use of a loop antenna
- Radiated Susceptibility
  - Electric Field:
    - » Testing is conducted in an EM shielded chamber with VISS connected to its support equipment with "flight-like" cabling and operated in its most sensitive mode (system ID, active, and passive)
  - Electrostatic Discharge (ESD):
    - » VISS is tested to detect susceptibilities to an ESD event due to S/C charging
    - » Several points along the exterior of VISS is subjected to a 3 millijoule discharge at a distance of 25 cm
    - » The discharge is generated using an induction coil sparker defined in MIL-STD-1541A

Radiated Emissions, Magnetic Field Limits



Radiated Susceptibility, Electric Field

Frequency Range		Field Strength (V/m)
	14 kHz - 30 MHz	10
	30 MHz - 10 GHz	5
	10 GHz - 18 GHz	20
(1)	2269.5 MHz	40
(1)	2288.5 MHz	40
(1)	5575 MHz (pulsed @ 2600 pps)	70
(2)	1280 Mhz to 1350 MHz	40
(2)	5400 Mhz to 5900 MHz	40

(1) These frequency bands and levels may change when the S/C and its transmit channels are selected

(2) Experiments should operate normally after exposure to the WTR launch site levels at the listed frequencies. These levels do not include any attenuation provided by the space vehicle fairing.

Additional testing at discrete telecommunication frequencies and levels will be performed once the S/C and launch vehicle are defined

PL Qualification Test
EMC (cont)

ESD Radiated Susceptibility

Gap Voltage	10 kV
Pulse Rate	1 per second
Distance between gap and equipment under test	25 cm
Discharge Energy	3 mJ

- DC Magnetic Characterization
  - Verify VISS compliance with the S/C's earth aspect sensor requirements
  - VISS is rotated about three axes at a specified distance from a magnetometer sensor to determine the maximum observable field
  - The data is normalized to an equivalent field at 1 meter
  - VISS magnetic flux density limit for testing is 50 nT at 1 m

Depending on the S/C selected, this requirement may change or not be necessary

APPENDIX II

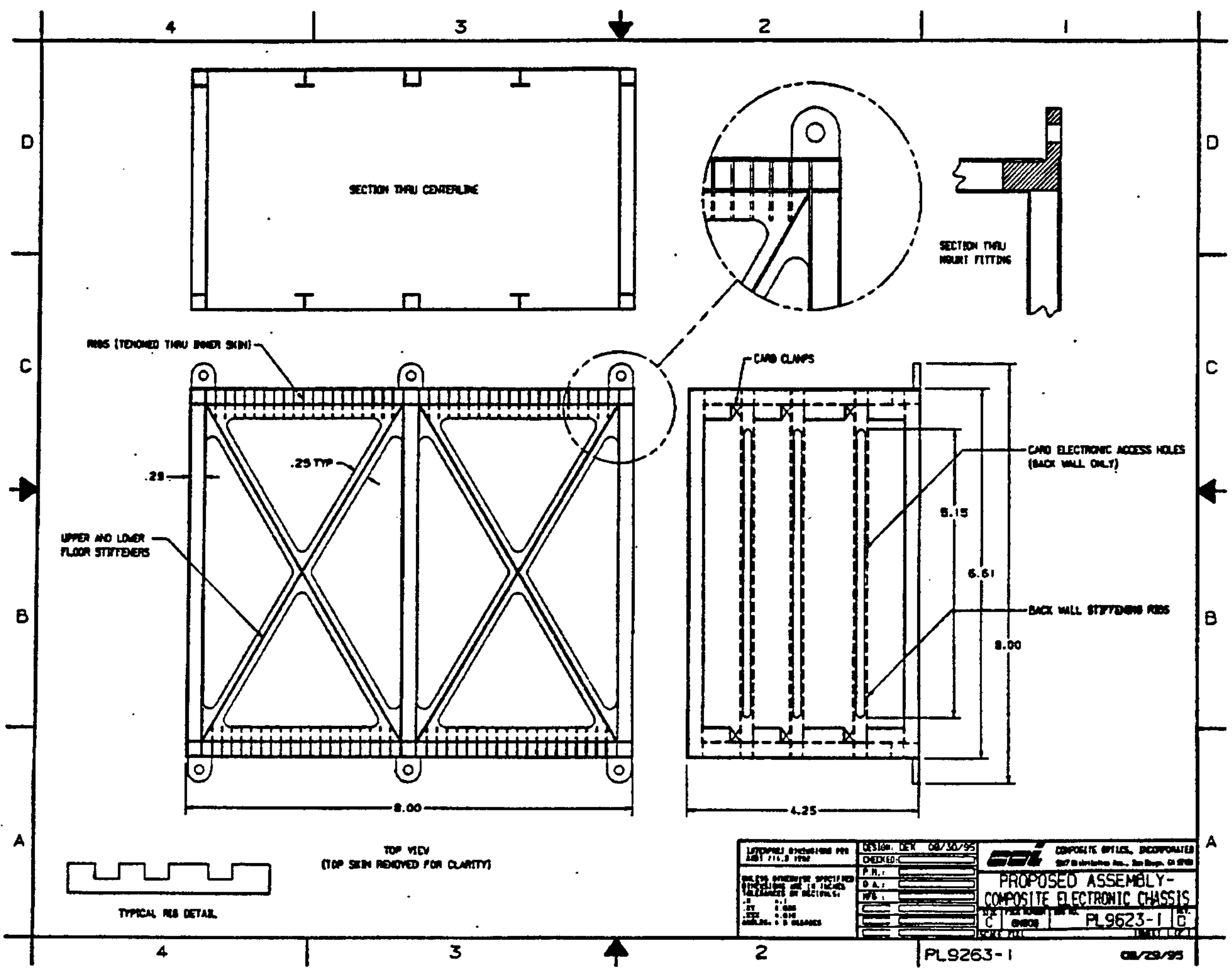


Figure 2. Composite Electronic Chassis

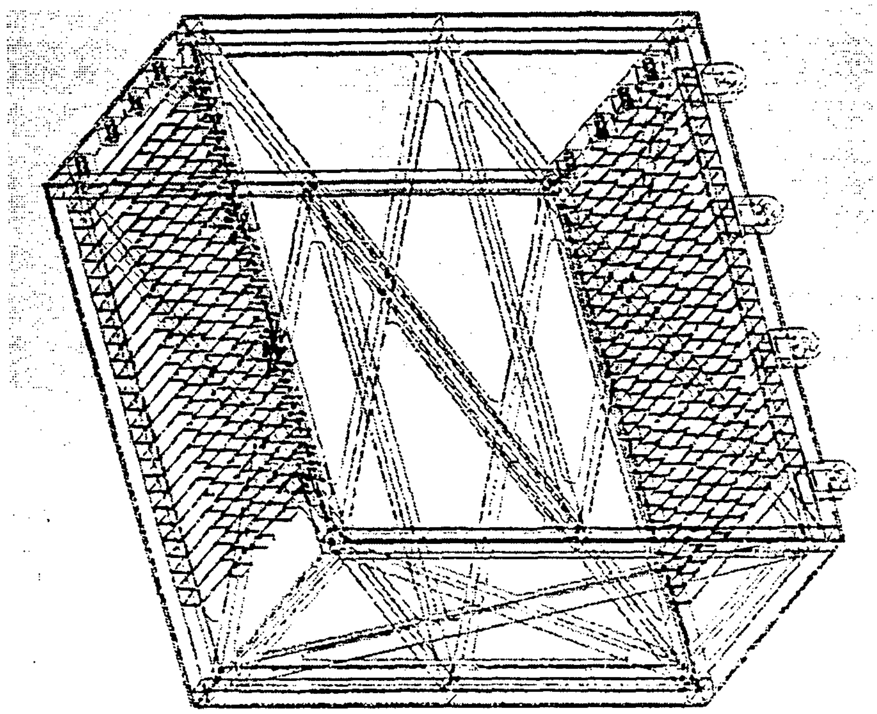


Figure 3. Chassis Structure

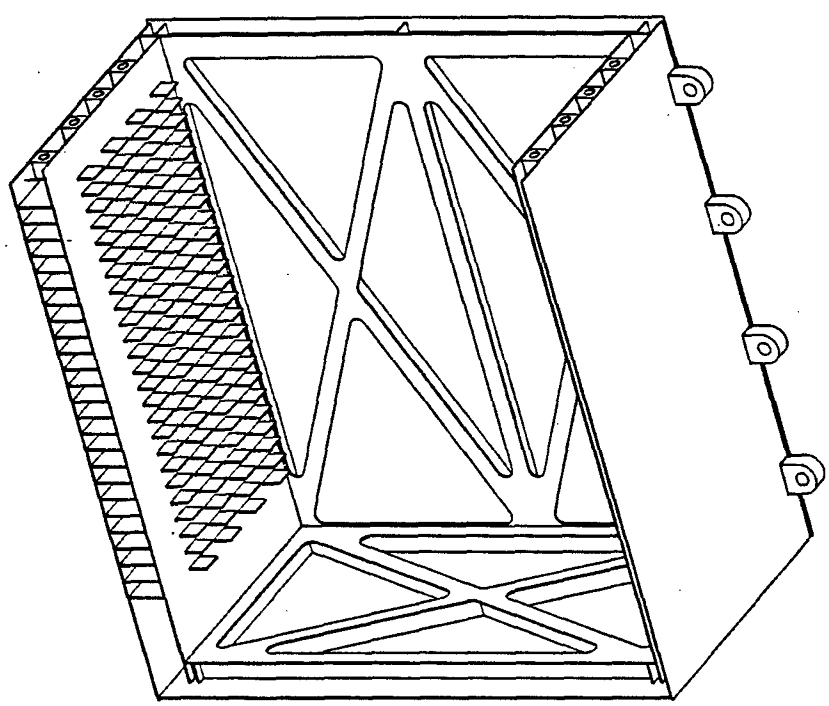


Figure 4. Chassis Structure with Outside Wall

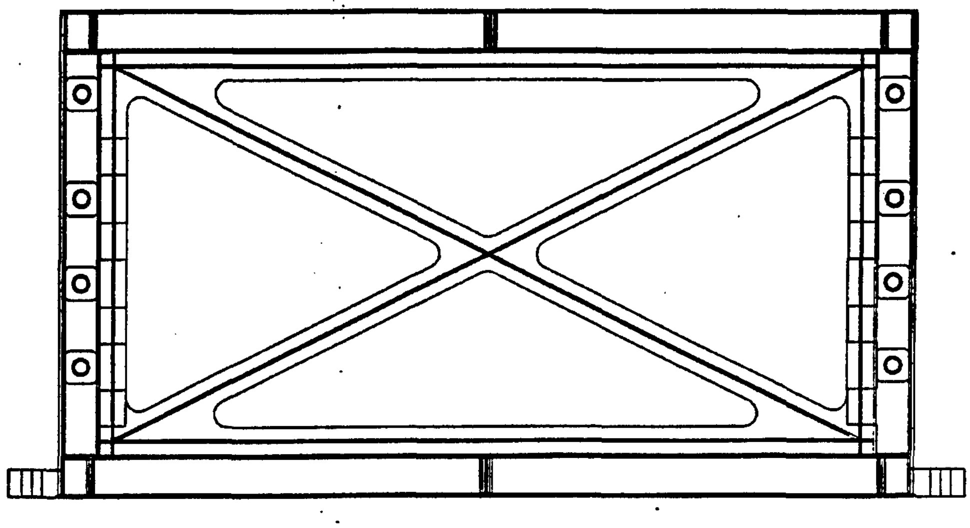


Figure 5. Chassis Structure - Front View

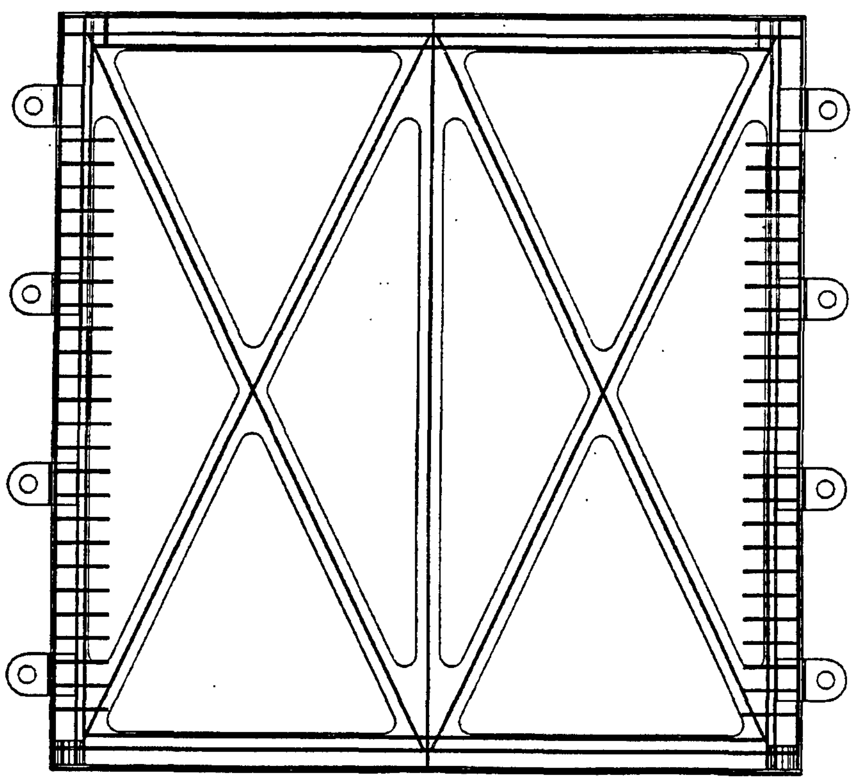


Figure 6. Chassis Structure - Top View

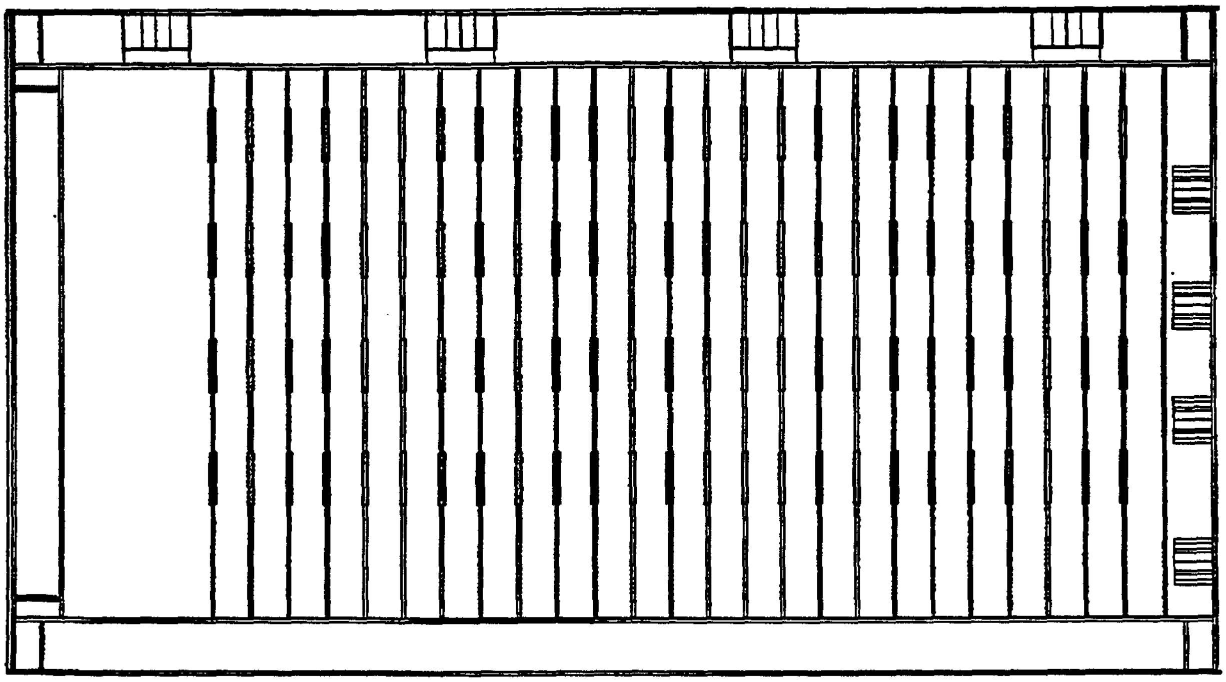


Figure 7. Side View Showing Heat Conducting Ribs

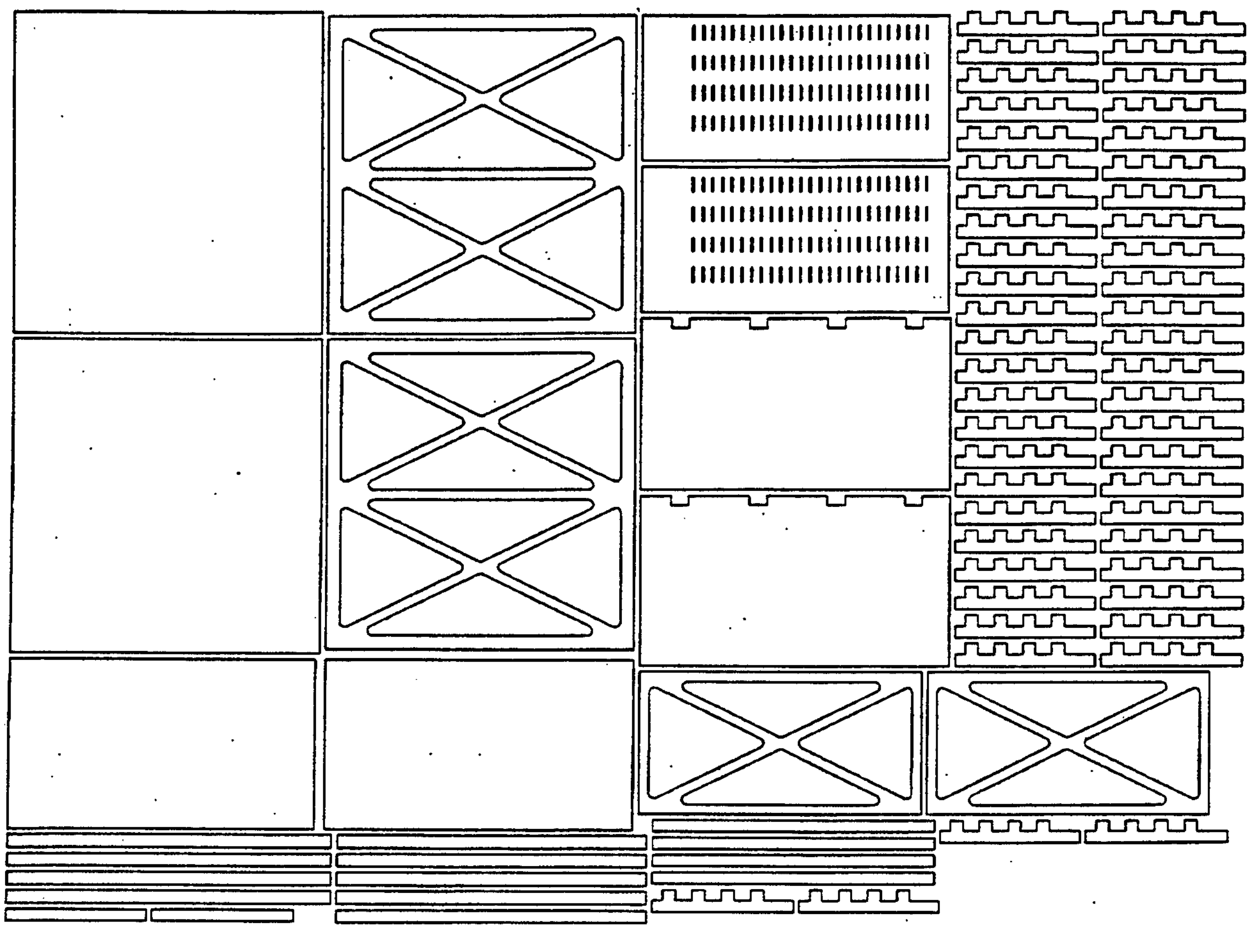


Figure 8. Layout for Waterjet Machining
(33"long by 24" wide)

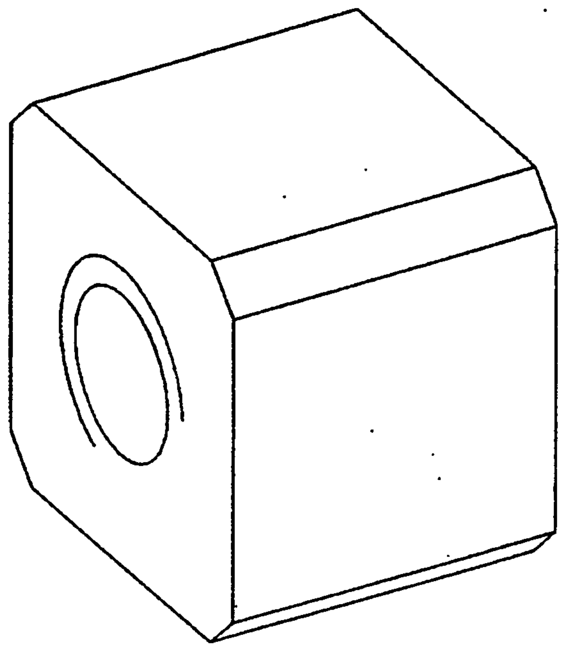


Figure 9. Cover Attachment Boss

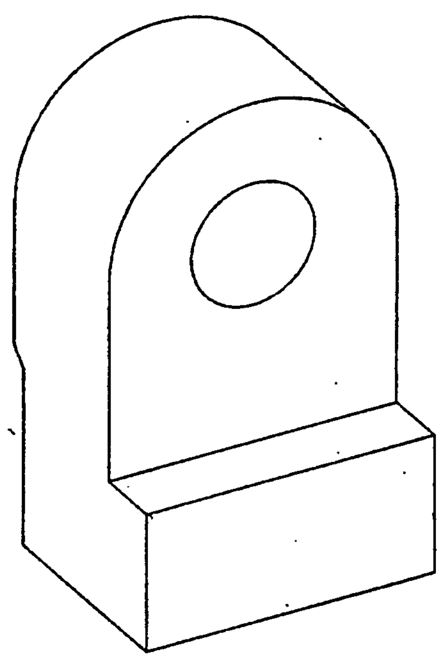


Figure 10. Enclosure Mounting Lug

APPENDIX III

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TecMation Associates, Ltd.
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Fort Collins, CO 80524-2253

Professional Engineering Services

FINAL REPORT
PO Number: 38086

PROJECT: Composite Electronic Structure Packaging **SBIR:** AF95-071 (Phillips Lab)

TITLE: Analysis Tasks per FY3592-95-10229-00 **DATE:** 04/22/96

Summary: The Phase I effort evaluated a P120/CE electronics chassis with three PWBs and six mount fittings. It weighed 11.74 lbs while the Aluminum configuration was 13.50 lbs with most of the reduction due to the composite chassis. The SBIR design was predicted to have acceptable thermal performance and positive stress margins of safety while being 70% lighter than the Al box. The chassis and PWB temperatures were similar to the results reported by Honeywell but unknown modeling parameters prevented a direct comparison. Trade studies with different carbon fibers indicated design modifications that would reduce temperatures by up to 36°C. The SBIR box was found ready to be developed into flight-qualified composite hardware in Phase II.

Discussion: The Phase I effort analyzed a generic composite electronics chassis, labeled SBIR, with estimated heat dissipation and mass distributions on the PWBs. The actual Honeywell design using Aluminum was not available in time for conversion. However, the differences between the two versions, as shown in Table 1, were such that a reasonable estimate of the composite chassis thermal and mechanical performance could be made when the results from each independent analysis were compared and the influence of modeling assumptions was understood.. The COSMOS/M finite element model had 1900 nodes and 3072 elements, mostly layered shells of P120/Cyanate Ester for the chassis (185 W/mK) and E-Glass/Polyimide for the cards (18 W/mK). The major features of the model are the ribbed side walls with card rails (Figure 1), the support frames and the cards (Figure 2), and the outer skins of the enclosure with the six mount fittings (Figure 3). The baseline configuration assumed a total of 50 watts of power and 10 lbs of electronics, allocated at 30%, 30%, and 40% on the top, middle, and bottom cards, respectively.

Table 1. Comparison of Electronic Enclosure Configurations

Design Parameter	SBIR-Gr/CE	HW-Aluminum
Size - L x W x H (in)	8.0 x 6.5 x 4.25	8.0 x 8.0 x 4.25
Weight - chassis (lb) - assy w/ PWBs	1.85 11.74	6.10 13.50
Max. Power Dissipation (w)	50	50
Number of PWB	3	4
Number of Mounting Points	6	8
Launch - MAC (g's) Loads - Random Vib (grms)	20 11.4	21 11.4
Safety Factors	1.25 yld, 1.40 ult	1.25 yld, 1.40 ult
Model Reference Temp (°C)	0.0	n/a
Operating Temperature (°C)	-5 to +30	-5 to +30
Clamping Load (lb)	125	125

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Results: Using this SBIR chassis model, several trade studies (Table 2) were performed to: 1) define the temperature changes from using different laminates, 2) indicate the benefits of using PWBs with a thin (0.010") thermal core of highly conductive material, and 3) compare these results with an earlier development effort [1] that had one card with only 3.2 watts of dissipated power. The effect of increasing fiber conductivity (and cost) reduced the chassis and card tem-

Table 2. Trade Studies of Possible Design Modifications

	MAXIMUM TEMPERATURES (°C)						
Laminate [W/mK]	K13C2U [162]		P120 [185]			K1100 [300]	
Location watts	50	3.2	50	core	3.2	50	3.2
Bottom Card	81.7	1.1	80.0	43.9	0.6	75.6	1.1
Middle Card	71.1	12.8	68.9	41.7	12.8	62.2	12.2
Top Card	74.4	1.7	71.7	44.4	1.1	63.9	0.6
Chassis Skin	23.9	2.2	21.1	20.6	1.7	13.3	1.1

peratures by 6 to 10°C for the three fibers studied. This indicates that little is gained from using K1100 unless the design is faced with the most demanding requirements. The primary influence on card temperature is the very low conductivity of the PWBs, about 10% of the chassis value. As shown in the center column, the PWBs with a P120 thermal core and the same rail interface resistance were 36°C (Power card) and 27°C (DSP and ASP cards) cooler without affecting the chassis, just making it conduct a heat load much closer to its capacity. Plots in °F (Figures 4 and 5) show the temperature variation on the SBIR model. This is typical behavior for all of the cases except that the maximum temperature changes. Figure 6 shows the low power card, indicating that the SBIR design could use any carbon fiber to make this case perform acceptably. The referenced study used a complex chassis open at both ends and tried a range of contact resistances to arrive at a decent correlation with their test data. Although their card temperature was much higher at 55°C and this varied little between the Aluminum and K1100 boxes, they did show the same influence of a card with thermal core. The card temperature reduced by about 15°C in both test and analysis. The poor thermal performance in [1] was certainly influenced by the open ends that disrupted the heat flow as indicated by the increased chassis temperature around the slots in the SBIR chassis, Figure 5.

Late in the program some thermal analysis data for the Honeywell chassis was received. This is shown in Table 3 for comparison with the SBIR chassis, without and with thermal core. The lack of a reference temperature for the HW analysis limits any direct comparisons of the two designs. Also, the change in chassis width, an increase in the number of mounts, the presence of external gap sensors, and the addition of another card modify the thermal characteristics. Finally, the treatment of contact resistances at the card rails and the mount fittings will alter the performance of each box. However, except for the reference temperature, most of the differences tend to balance out so that some general conclusions can be made. Card temperatures are similar and follow the same trend for the different card types. Not having as high a peak card temperature is largely due to the dissipated heat being uniformly distributed over the card while the flange temperature difference reflects the unknown HW reference temperature and the different mounting interface treatment.

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Table 3. Comparison of Thermal Analysis - Maximum Temperatures (°C)

Enclosure Location	SBIR-Gr/CE		HW-Aluminum
PWB Mat'l	Gl/PI	w/ core	Glass/PI
Flange	13.0	16.8	59.1
Chassis	21.1	20.6	64.2
Power PWB	80.0	43.9	90.1
DSP PWB	68.9	41.7	87.1
ASP 16 PWB	n/a	n/a	82.9
ASP 12 PWB	71.7	44.4	94.3
MCP Case	n/a	n/a	101.4
Gap Sensor Case	n/a	n/a	64.9

The final part of the analysis was to determine the structural integrity of the SBIR chassis. The critical stress results are summarized in Table 4. Critical stress was determined by combing the effect of clamping load with the highest acceleration result in one of the model axes. Stress plots for clamping loads (Figures 7a and 7b), 1-g X acceleration (Figures 8a and 8b), 1-g Y acceleration (Figure 9), and 1-g Z acceleration (Figure 10) are included. High margins of safety were found for this conservative SBIR box design. Upgrading this to the Honeywell design should present no difficulty once their final design parameters (i.e. box size, electronic component weights, operating temperature limits, and design load factors) are specified.

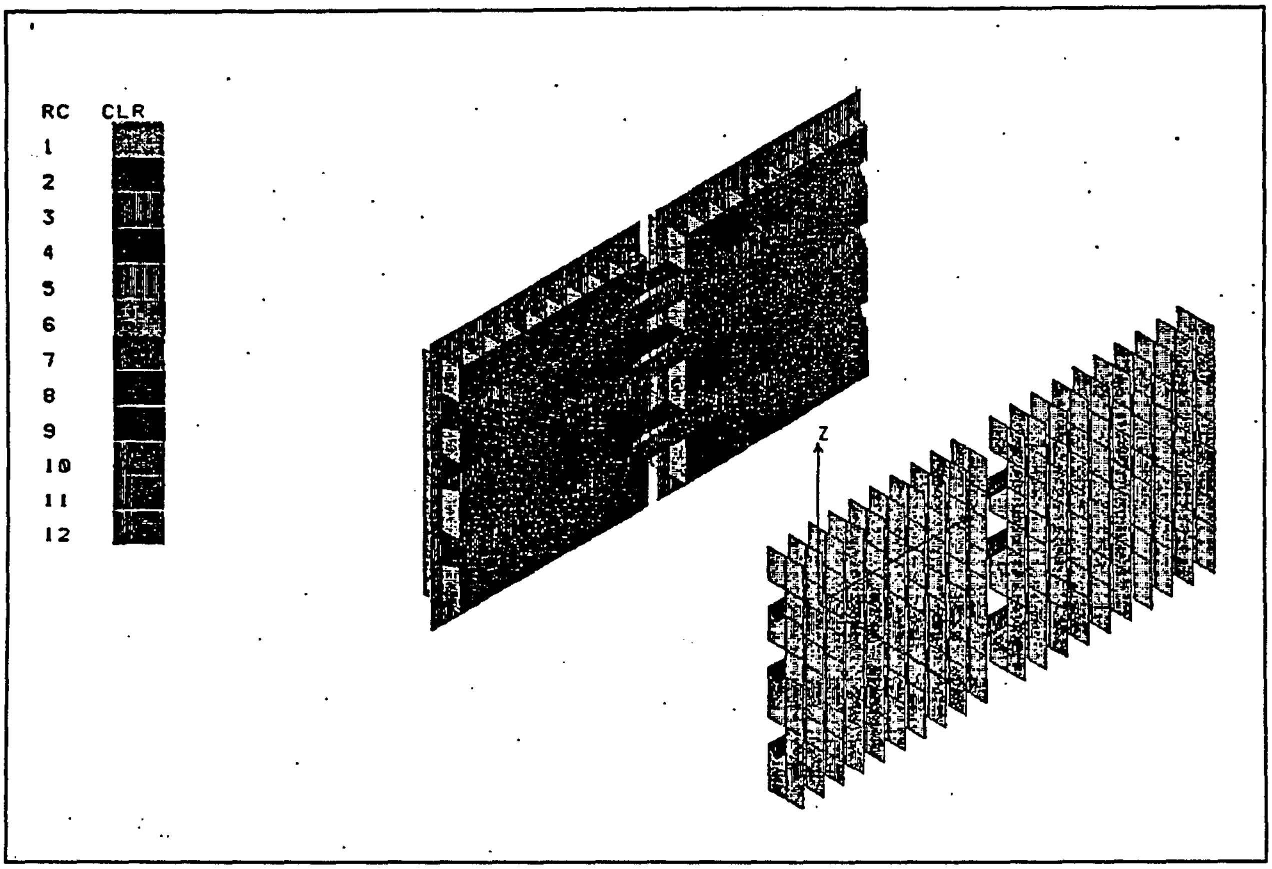
Table 4. SBIR Enclosure - Critical Stress Summary (psi)

Location (mat'l)	Clamp Load Stress	20 g Stress	Critical Stress	Design Allowable	Margin of Safety yield	ultimate
Box Skin (P120/CE)	913	5820	6733	29500	2.51	2.13
Bottom PWB (Gl/PI)	200	4100	4300	36800	5.85	5.11
Fitting Pull-out (Adhesive)	173	860	1033	2500	0.94	0.74
Mount Fitting (6061-T6)	500	4320	4820	34000	4.64	4.04

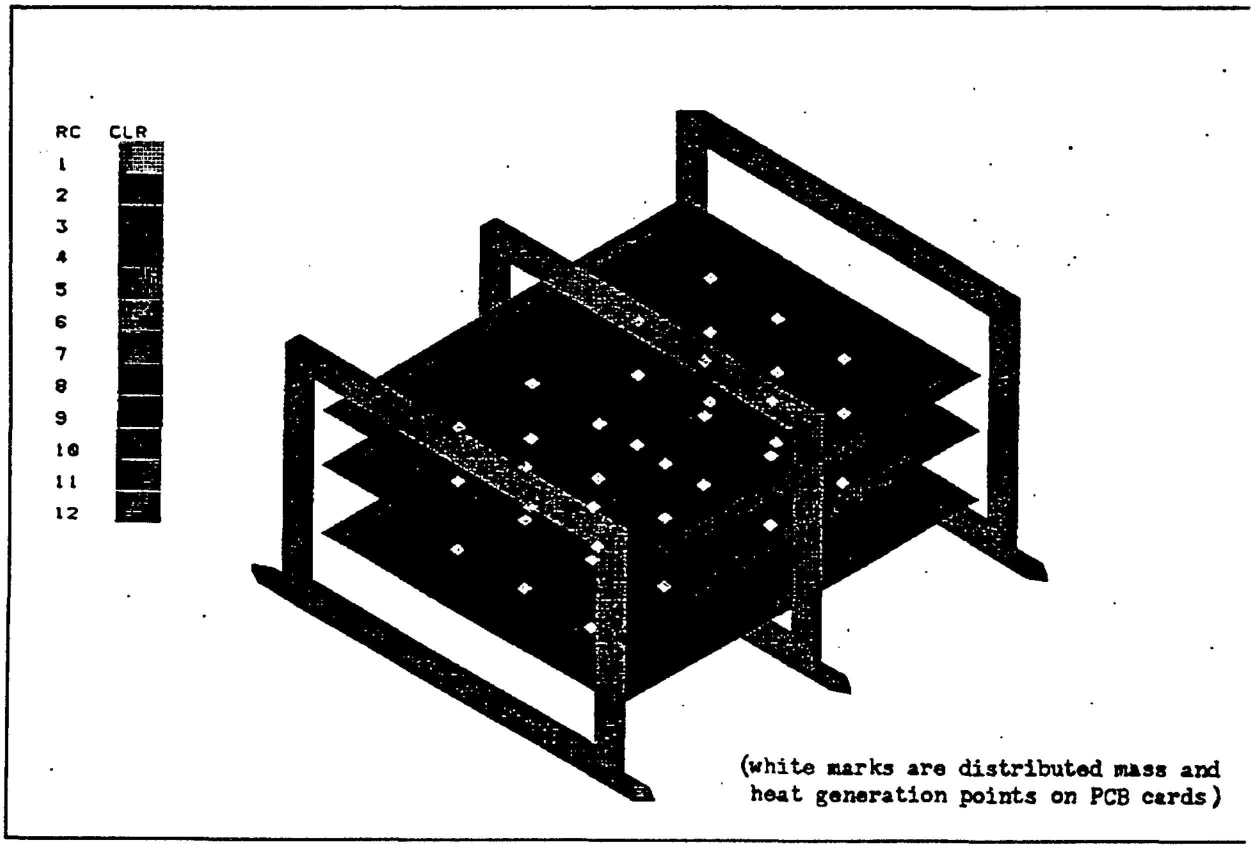
Conclusions: Both the thermal and mechanical performance predicted for the SBIR chassis indicate that flight-qualified composite hardware can be delivered. The open issues are electromagnetic compatibility and radiation shielding which require additional testing and development. This is scheduled for Phase II.

References:

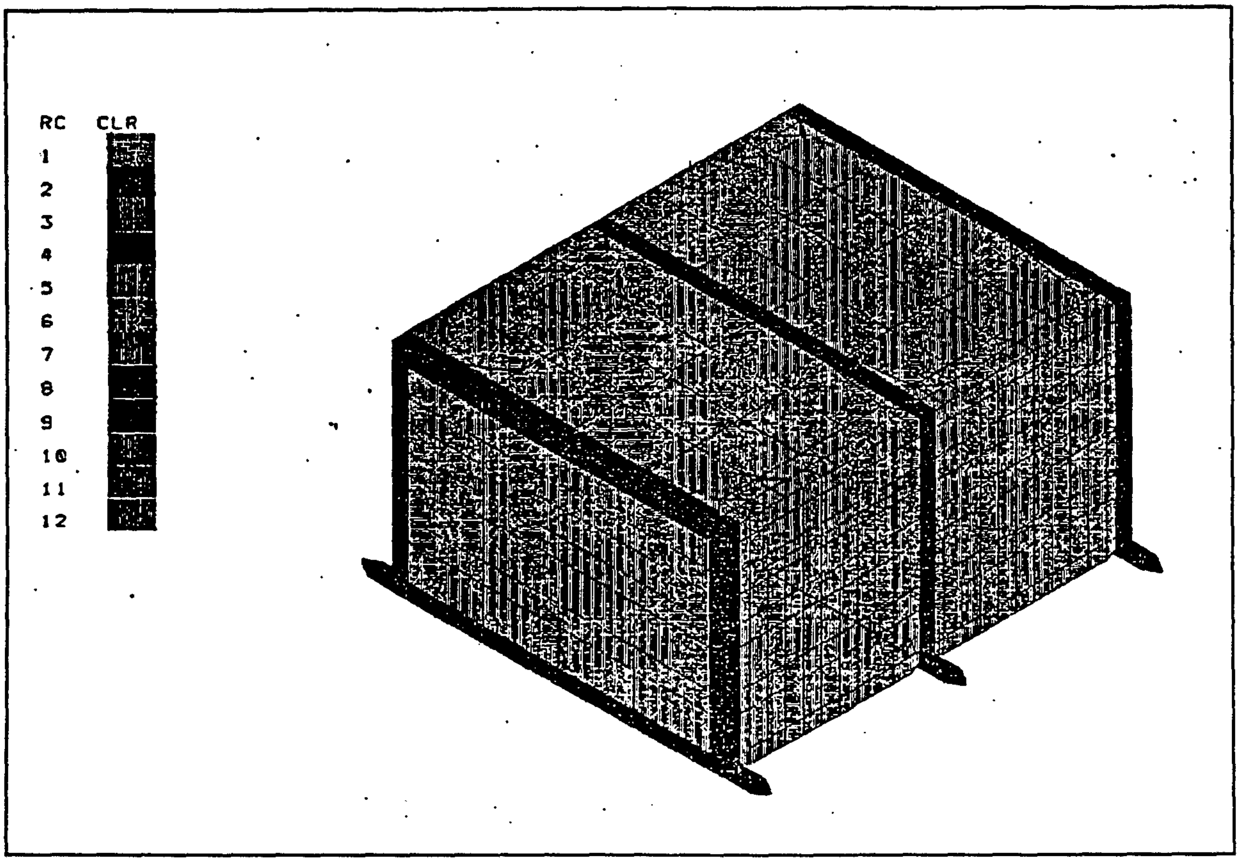
1. S.G. Beard et al., "Thermal Vacuum Laboratory Tests and 3-D Thermal Analysis of a K1100X Graphite Composite Satellite Electronics Box", Sandia Lab Memo dated 4/25/95.



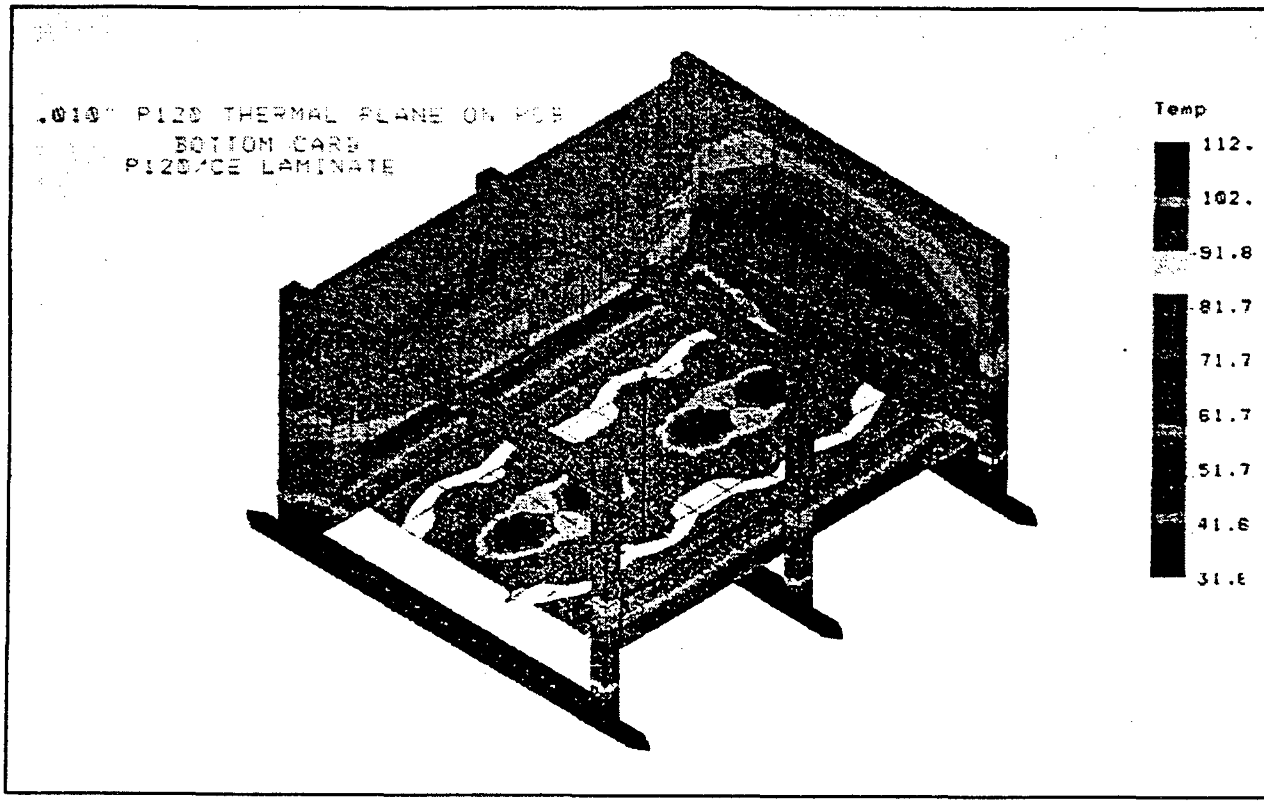
Appendix III, Figure 1. Ribbed Side Walls with Card Rails



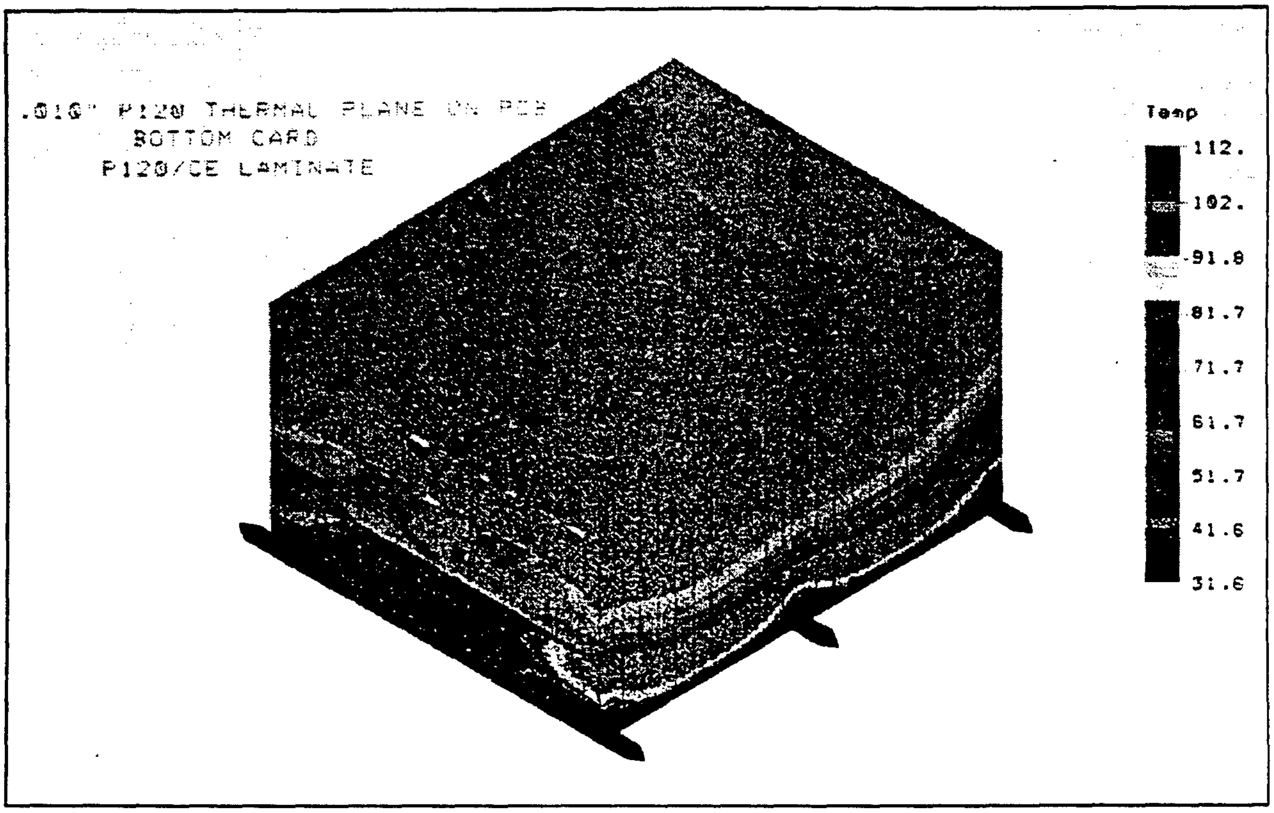
Appendix III, Figure 2. Frame and PCB Cards



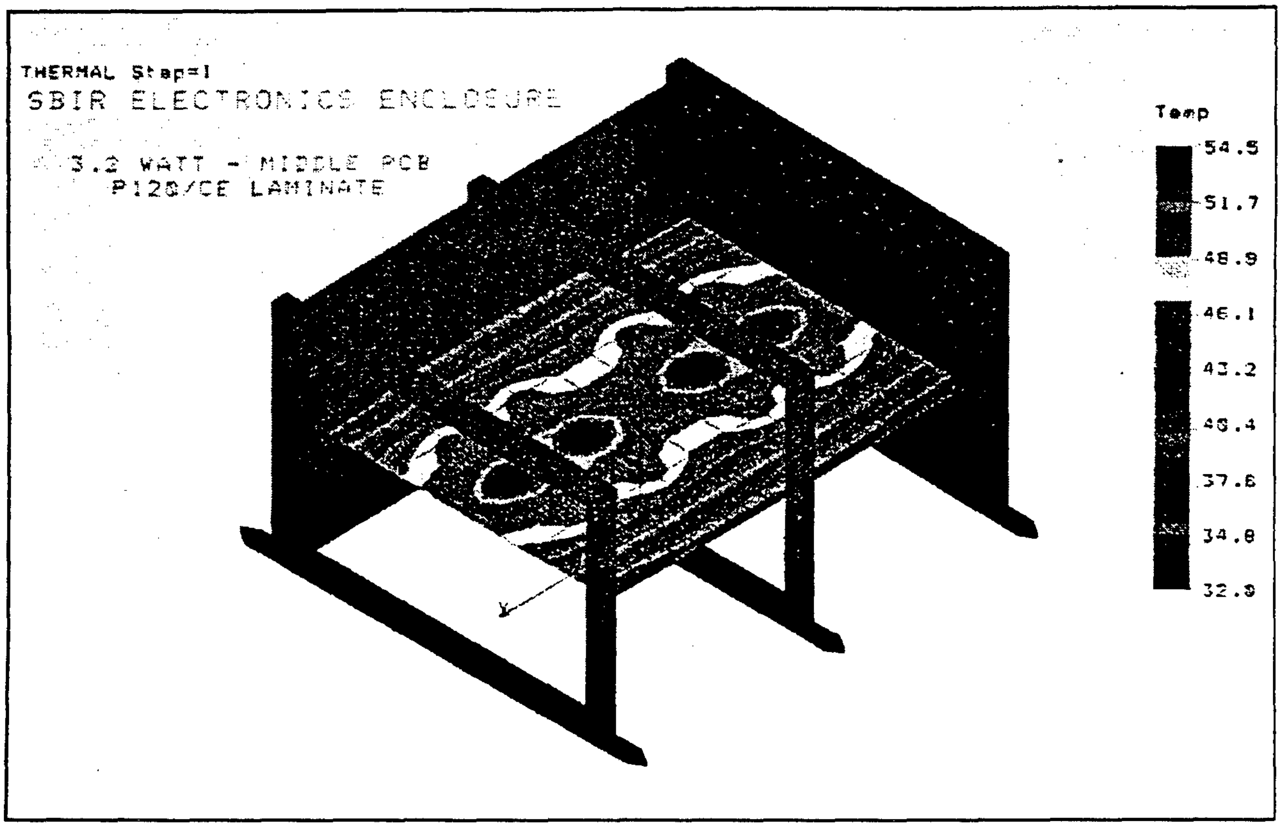
Appendix III, Figure 3. Outer Skin of Enclosure with Mount Fittings



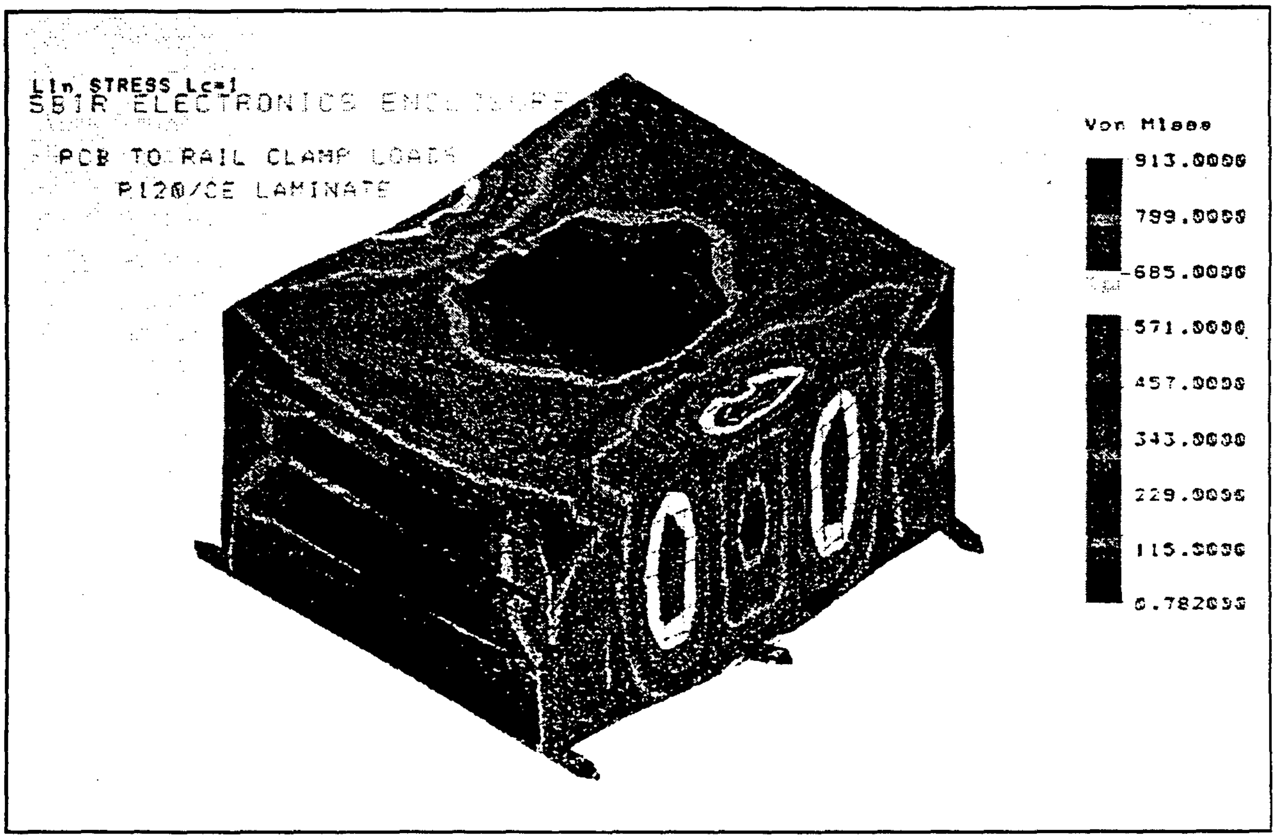
Appendix III, Figure 4. SBIR Electronics Enclosure



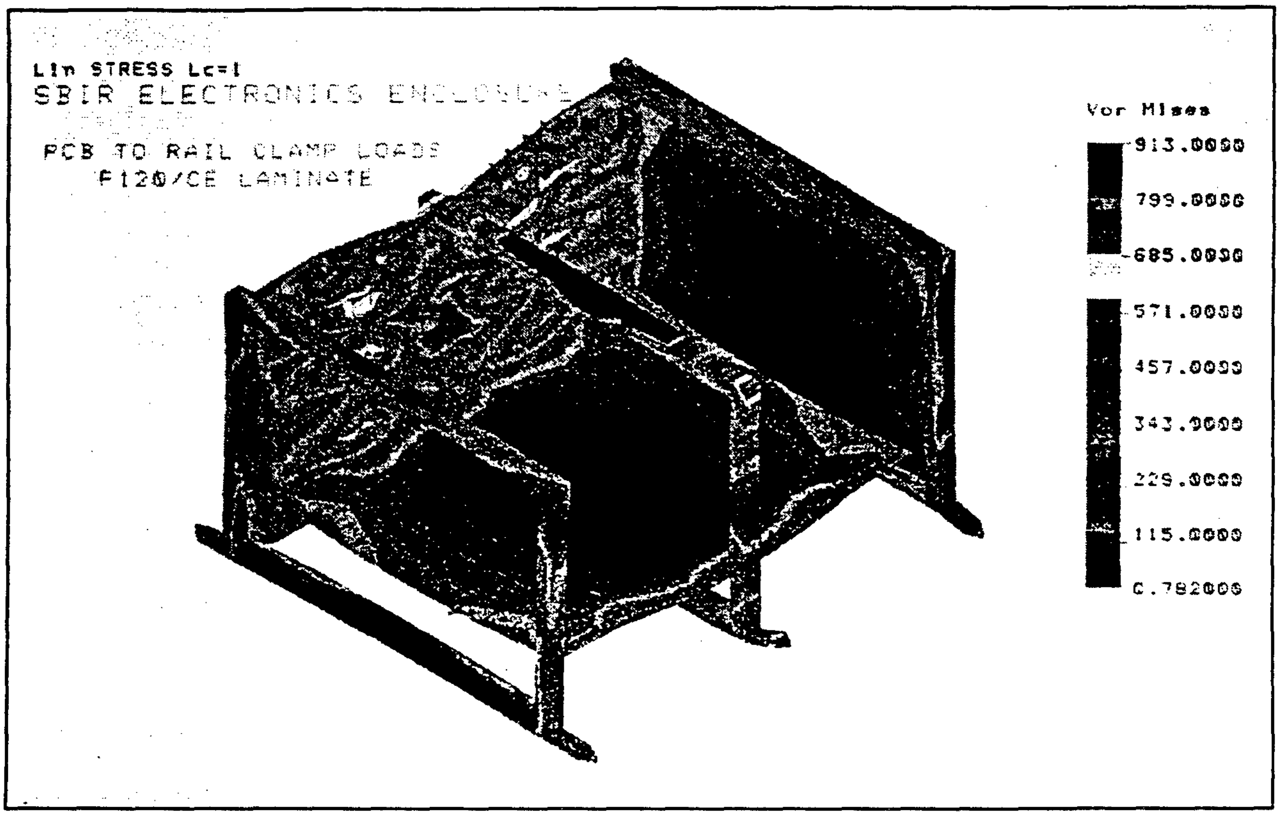
Appendix III, Figure 5. SBIR Electronics Enclosure



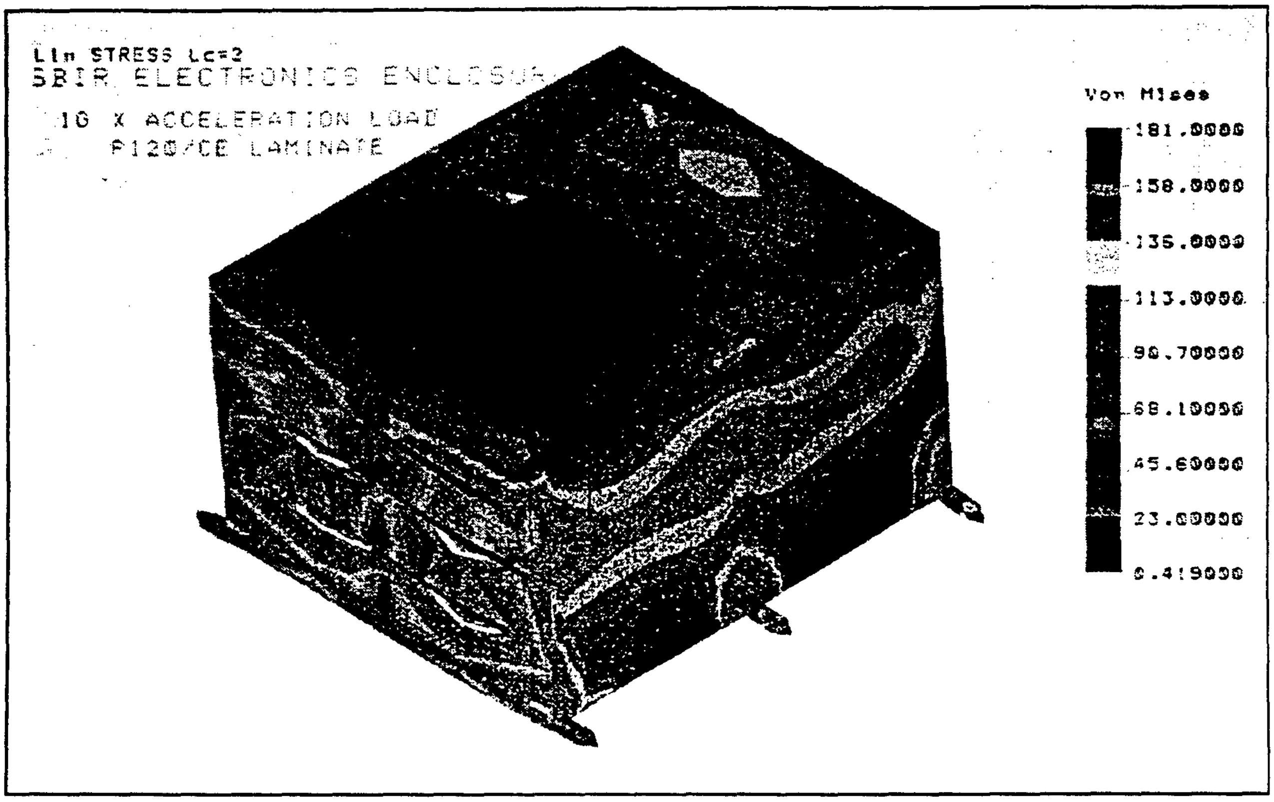
Appendix III, Figure 6. SBIR Electronics Enclosure



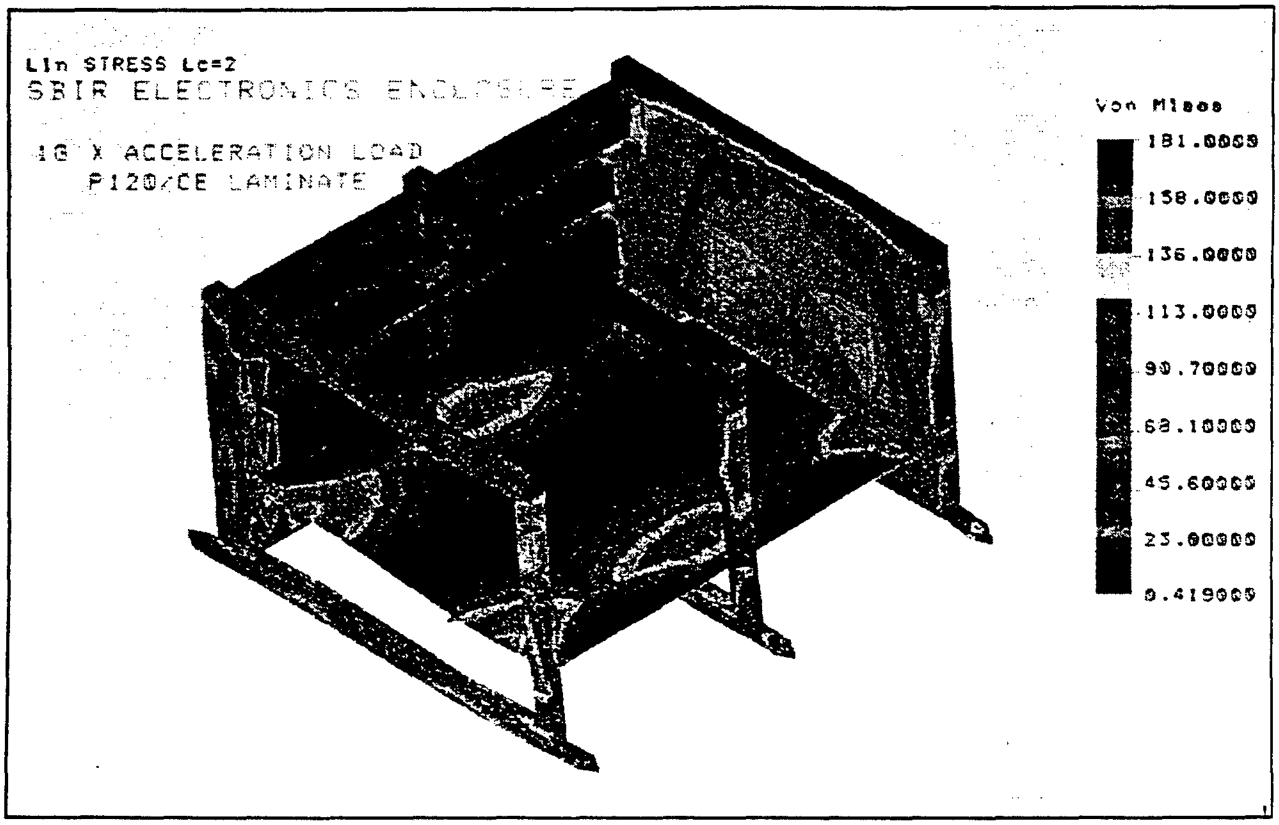
Appendix III, Figure7a. Outer Skin



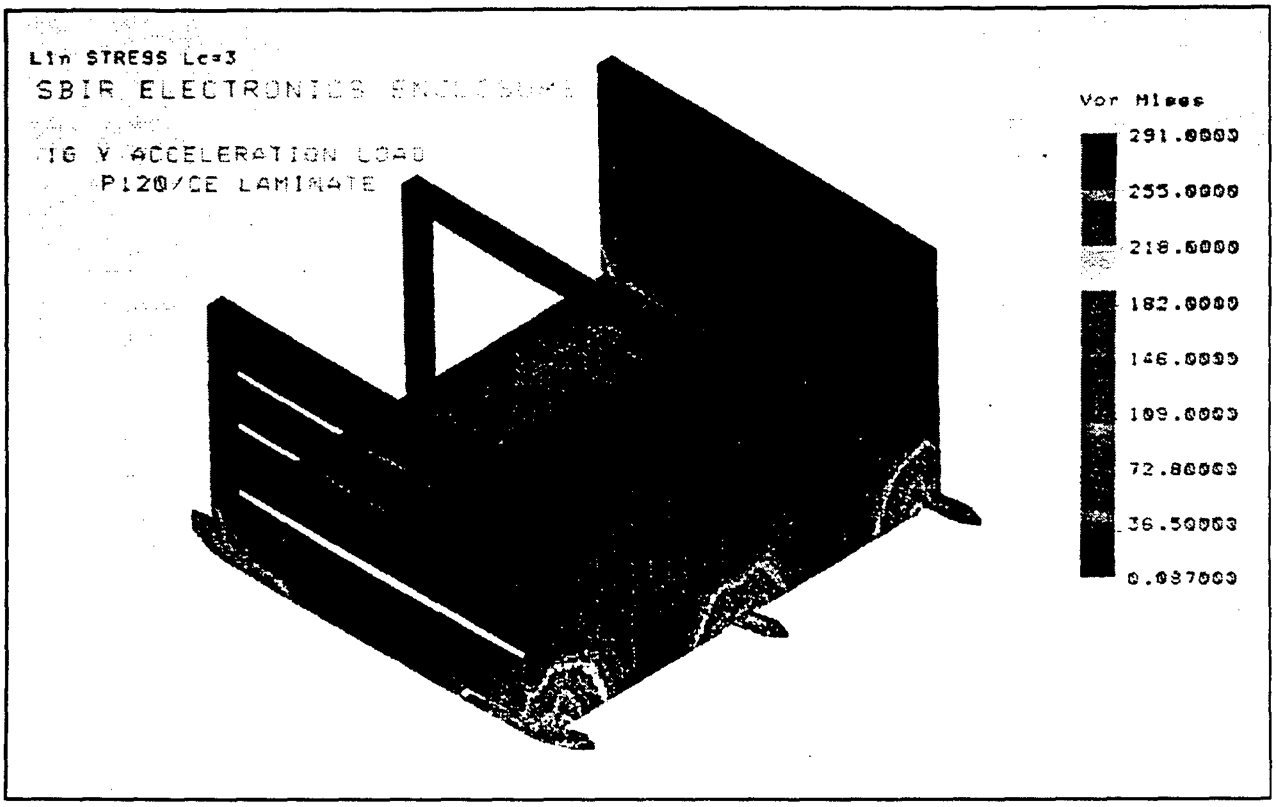
Appendix III, Figure7b. Cut-away for Inner Skin



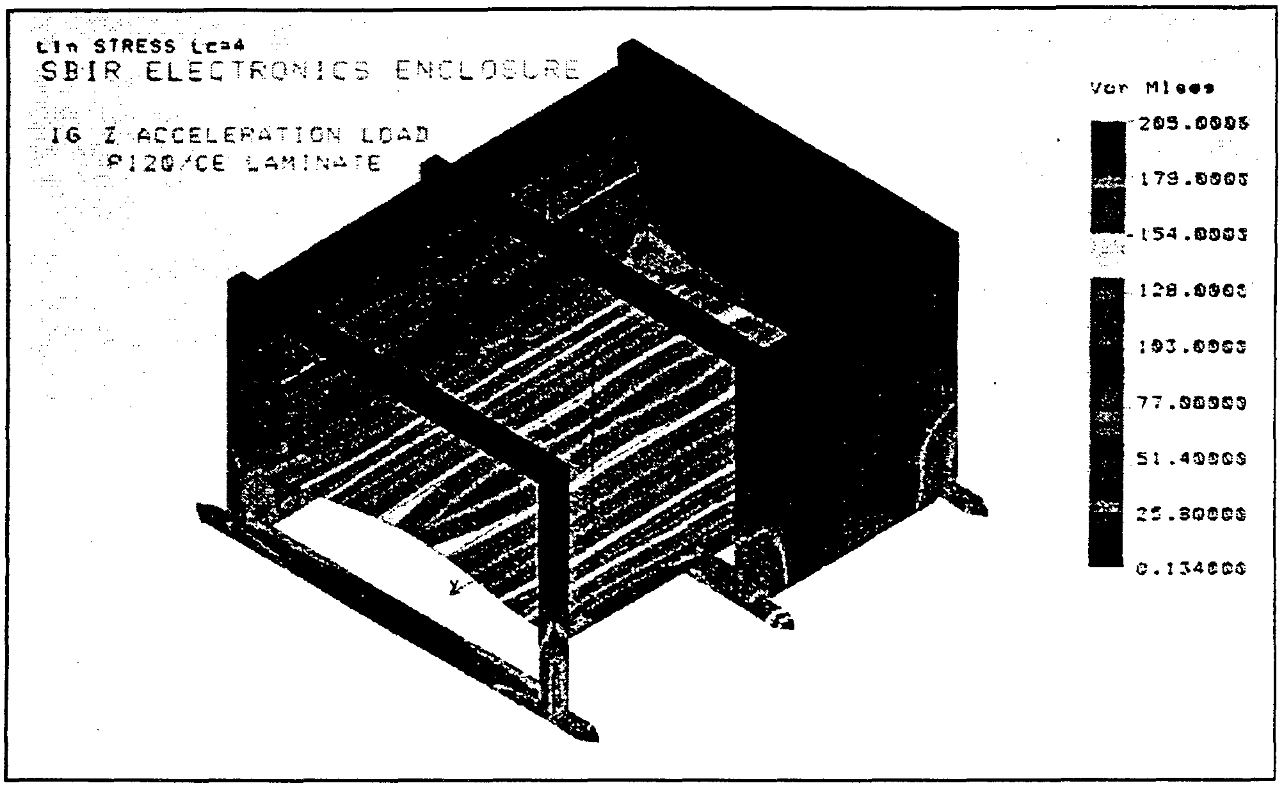
Appendix III, Figure 8a. Outer Skin



Appendix III, Figure 8b. Cut-away for Inner Skin



Appendix III, Figure 9. Cut-away with Side Skin



Appendix III, Figure 10. Cut-away with Bottom PWB

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